35. (New) The method as recited in claim 31, wherein each of the of the selected type of decoupling capacitor has a capacitance value, a mounted resistance value, and a resonant frequency value.

REMARKS

Claims 1-15 and 17-30 were pending in the application. Claims 8 and 17 have been amended. Claims 31-35 have been added. Therefore claims 1-15 and 17-35 are pending in the application.

35 U.S.C. § 103 Rejection:

Claims 1-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Harada, et al., U.S. Patent 6,198,362, in view of Roy et al., "ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications" and Novak, "Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination". Claim 16 has been cancelled, and thus Applicant believes its rejection to now be moot. With respect to the remaining claims, Applicant respectfully traverses this rejection.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. Harada teaches a printed circuit board. A top layer power supply pattern and a top layer ground pattern are formed. The top layer power supply pattern and the top layer ground pattern are connected to a power supply layer and a ground layer through a plurality of viaholes, respectively. A plurality of capacitors or a plurality of capacitor resistor series circuits are disposed at predetermined intervals between the top layer power supply pattern and the top layer ground pattern.

Roy teaches that power distribution system noise affects computer product timing performance, signal integrity and electromagnetic interference. Between 1 MHz and 1 GHz, the primary means of reducing power distribution noise is with ceramic decoupling

capacitors. To achieve a certain target impedance, it is important to characterize the ESR of ceramic decoupling capacitors as they directly determine the number of capacitors required on the board. Another factor which determines the capacitance value of decoupling capacitors is the ESL (inductance) associated with capacitors mounted on a PCB.

Novak teaches that power and ground planes should exhibit low impedance over a wide range of frequencies. Parallel ground and power planes in multiplayer printed-circuit boards exhibit multiple resonances which increase the impedance and also the radiation from the edge of the board. Resistive termination along the board edges reduces the resonance peaks.

In contrast, Applicant teaches an electrical power distribution structure and methods to achieve a target electrical impedance therefor. Independent claim 1 recites, in pertinent part:

> "wherein the mounted inductance L_m of each of the n capacitors is less than or equal to $(0.2 \cdot n \cdot \mu_0 \cdot h)$, and wherein μ_0 is the permeability of free space, and wherein h is a distance between the planar conductors" (Emphasis added).

Similarly, independent claim 8 recites, in pertinent part:

> "wherein the mounted inductance L_m is less than or equal to the inductance of the electrical power distribution structure L_p" (Emphasis added).

Independent claim 17 also recites a similar combination of features.

Neither Harada, Novak, nor Roy teach or suggest this combination of features. In particularly, none of the cited references teaches or suggests selecting capacitors such that their mounted inductance is less than or equal to the inductance of the electrical power distribution structure. Furthermore, Applicant submits that neither Novak nor Roy

provide any teaching, suggestion, or motivation to modify Harada in order to obtain the combinations of features recited in the independent claims.

In the Office Action, referring to the definition of mounted inductance L_m in claim 1, the Examiner states: "This recitation is merely describing a property of the capacitor, which is inherent to the device of Harada et al. ...". Applicant respectfully disagrees with this statement, and asserts that a mounted inductance that is less than or equal to an inductance of an electrical power distribution structure is not an inherent property of a capacitor.

Patentability of the Added Claims:

The present amendment adds new claims 31-35. Claim 31 is an independent claim, while claims 32-35 depend upon claim 31. Applicant submits that claims 31-35 recite combinations of features not taught or suggested in the prior art. Support for claims 31-35 may be found throughout the specification. For example, various features of claim 31 are supported in the specification starting at line 17 of page 24 through line 14 of page 27.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Conley, Rose, & Tayon, P.C. Deposit Account No. 05-1505/5181-62800/BNK.

Also enclosed herewith are the following items:

- [x] Return Receipt Postcard
- [ ] Petition for Extension of Time
- [ ] Request for Approval of Drawing Changes
- [ ] Notice of Change of Address
- [ ] Check in the amount of $ for fees ( ).
- [ ] Other:

Respectfully submitted,

B. Noel Kivlin
Reg. No. 33,929
ATTORNEY FOR APPLICANT(S)

Conley, Rose & Tayon, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 476-1400

Date: 7-19-02

MARKED UP COPIES OF THE AMENDED CLAIMS

8. (Twice Amended) A method for achieving a target electrical impedance Z_t in an electrical power distribution structure including a pair of parallel planar conductors separated by a dielectric layer, the method comprising:

determining a separation distance h between the parallel planar conductors required to achieve the target electrical impedance Z_t;

determining a required number n of a selected type of discrete electrical capacitor dependent upon an inductance of the electrical power distribution structure L_p and a mounted inductance L_m of a representative one of the selected type of discrete electrical capacitor when electrically coupled between the planar conductors, wherein $n \geq 2$, wherein the mounted inductance L_m is less than or equal to the inductance of the electrical power distribution structure L_p;

using the target electrical impedance Z_t to determine a required value of mounted resistance $R_{m\text{-}req}$ for the n discrete electrical capacitors;

selecting the required number n of the selected type of discrete electrical capacitor, wherein each of the n capacitors has a mounted resistance R_m substantially equal to the value of required mounted resistance $R_{m\text{-}req}$; and

electrically coupling the n discrete electrical capacitors between the planar conductors.

17. (Amended) A method for achieving a target electrical impedance Z_t in an electrical power distribution structure including a pair of parallel planar conductors separated by a dielectric layer, the method comprising:

determining a first required number n_1 of a selected type of discrete electrical capacitor dependent upon an inductance of the electrical power distribution structure L_p and a mounted inductance L_m of a representative one of the selected type of discrete electrical capacitor when electrically coupled between the planar conductors, wherein $n_1 \geq 2$, and wherein the mounted inductance L_m of each of the selected type of discrete electrical capacitor is less than or equal to the inductance of the electrical power distribution structure L_p;

determining a second required number n_2 of the selected type of discrete electrical capacitor dependent upon a distance d_p around an outer perimeter of the electrical power distribution structure and a spacing distance S between adjacent discrete electrical capacitors, wherein $n_2 \geq 2$;

performing the following if $n_2 \geq n_1$:

using the target electrical impedance Z_t to determine a required value of mounted resistance $R_{m\text{-}req}$ for n_2 of the discrete electrical capacitors;

selecting n_2 of the discrete electrical capacitors, wherein each of the n_2 capacitors has a mounted resistance R_m substantially equal to the value of required mounted resistance $R_{m\text{-}req}$; and

electrically coupling the n_2 discrete electrical capacitors between the planar conductors along an outer perimeter of the parallel planar conductors.